

65705 U.S. PRO  
09/583097  
00/02/99

Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

RS SCANNED <u>Am'</u> Q.A. <u>CH</u>	O.I.P.E. PATENT DATE
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APPLICATION NO. 09/583097	CONT/PRIOR D	CLASS 712	SUBCLASS 215	ART UNIT 2183	EXAMINER
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Marc Tremblay

Huis van

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Groupings logic circuit in a pipelined superscalar processor

PTO-2040  
12/99

ISSUING CLASSIFICATION													
ORIGINAL					CROSS REFERENCE(S)								
CLASS		SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
INTERNATIONAL CLASSIFICATION													

☐ Continued on Issue Slip Inside File Jacket

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ _____ _____				<b>ISSUE FEE</b>	
	_____ (Primary Examiner) (Date)			Amount Due	Date Paid
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	
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